161

2811

PTO/SB/21 (08-03)
Approved for use through 08/30/2003. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/821,636
Filing Date	March 29, 2001
First Named Inventor	Hiroyuki Ikeda
Art Unit	2811
Examiner Name	Thien F. Tran
Attorney Docket Number	075834.00064

Total Number of Pages in This Submission

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
- ☐ Fee Attached
- ☐ Amendment/Reply
- ☐ After Final
- ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
- ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☑ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance communication to Technology Center (TC)
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):

Post Card

Remarks

The Commissioner is hereby authorized to charge any fees due or to credit any overpayment to Deposit Account No. 50-1794.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Robert J. Depke, Holland & Knight LLC 131 South Dearborn Street, 30th Floor, Chicago, IL 60603
Signature	
Date	4/8/04

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Typed or printed name	Robert J. Depke (Reg. No. 37,607)		
Signature		Date	4/8/04

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.:	09/821,636	**Confirmation No.:**	5712
Applicant:	Hiroyuki Ikeda		
Filed:	March 29, 2001		
TC/A.U.:	2811		
Examiner:	Thien F. Tran		
Docket No.:	075834.00064		
Customer No.:	33448		

PETITION TO SHOW TIMELY FILING

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

S I R:

On November 18, 2003 the patent office mailed a Notice of Abandonment in the above referenced United States patent application as a result of a purported failure to respond to the outstanding office action dated March 19, 2003.

Contrary to these assertions, the undersigned submits that Applicant submitted a timely response which was actually received by the patent office in a timely manner as detailed below. Accordingly, Applicant request that the abandoned status of this application be withdrawn and the Examiner now consider Applicant's response to the outstanding office action.

In support of this petition the undersigned notes that Applicant filed a timely Request for Continued Examination prior to expiration of the six-month period with the requisite fees

and request for extension of time to respond as well as a cover sheet referencing the express mailing label and a certificate of mailing. A copy of each these documents is attached along with the preliminary amendment accompanying the RCE. The documents were submitted via express mail on September 19, 2003 via mailing label number ET910403511US.

The patent office apparently received the Request for Continued Examination as reflected by the September 19, 2003 entry from the PAIR file contests history record, a copy of which is attached hereto. Additionally, Applicant has attached a copy of the stamped postcard receipt reflecting receipt in the patent office on September 19, 2003 of the response.

In light of the foregoing, Applicant submits that a timely response was actually filed and indeed received by the patent office in a timely manner and accordingly, Applicant requests that the Examiner withdraw the abandoned status of this application and now consider the outstanding office action.

Respectfully submitted,

Date: April 8, 2004

(Reg. #37,607)

Robert J. Depke
HOLLAND & KNIGHT LLC
131 S. Dearborn, 30th Floor
Chicago, Illinois 60603
Tel: (312) 263-3600
Attorney for Applicant

App. No. 09/821,636
Petition to Show Timely Filing dated April 8, 2004

CERTIFICATE OF MAILING

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Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney for Applicant

9 571 272
1615

United States Patent and Trademark Office

PATENT APPLICATION INFORMATION RETRIEVAL

Search results for application number: 09/821,636			
Application Number:	09/821,636	Customer Number:	33448
Filing or 371(c) Date:	03-29-2001	Status:	Abandoned -- Failure t Respond to an Office A
Application Type:	Utility	Status Date:	11-17-2003
Examiner Name:	TRAN, THIEN F	Location:	TECH CENTER 2800 - CENTRAL FILE CP-4 4
Group Art Unit:	2811	Location Date:	11-25-2003
Confirmation Number:	5712	Earliest Publication No:	US 2001-0030323 A1
Attorney Docket Number:	09792909-4795	Earliest Publication Date:	10-18-2001
Class/ Sub-Class:	257/059	Patent Number:	-
First Named Inventor:	Hiroyuki Ikeda, Kanagawa, (JP)	Issue Date of Patent:	-
Title Of Invention:	Thin film transistor apparatus		

Foreign Priority | Continuity Data

File Contents History

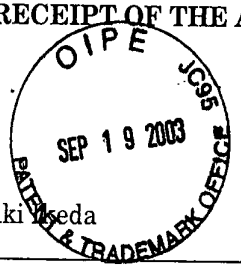
Number	Date	Contents Description
22	11-18-2003	Mail Abandonment for Failure to Respond to Office Action
21	11-17-2003	Abandonment for Failure to Respond to Office Action
20	09-19-2003	Workflow - Request for RCE - Begin
19	03-19-2003	Mail Final Rejection (PTOL - 326)
18	03-19-2003	Final Rejection
17	01-10-2003	Date Forwarded to Examiner
16	01-03-2003	Response after Non-Final Action
15	10-24-2002	Mail Non-Final Rejection
14	10-21-2002	Non-Final Rejection
12	07-29-2002	Date Forwarded to Examiner
11	07-15-2002	Response to Election / Restriction Filed
10	07-25-2002	Correspondence Address Change
9	07-25-2002	Change in Power of Attorney (May Include Associate POA)
8	06-07-2002	Mail Restriction Requirement
7	06-06-2002	Requirement for Restriction / Election
6	12-11-2001	Case Docketed to Examiner in GAU
5	07-02-2001	Case Docketed to Examiner in GAU
4	06-01-2001	Application Dispatched from OIPE
3	06-01-2001	Correspondence Address Change
2	04-19-2001	IFW Scan & PACR Auto Security Review

1	03-29-2001	Initial Exam Team nn

HON. COMMISSIONER OF PATENTS
ALEXANDRIA, VA 22313-1450

SIR:

PLEASE APPLY A RECEIPT STAMP HERETO AND MAIL TO ACKNOWLEDGE RECEIPT OF THE ATTACHED:



Express Mail Certificate, PTO/SB/30
Request for Continued Examination Transmittal, Prelim. Amendment with Time Extension Request, Fee Transmittal, $750 & $930 checks

Hiroyuki Ueda

APPLICANT

TYPE OF DOCUMENT(S):

September 17, 2003

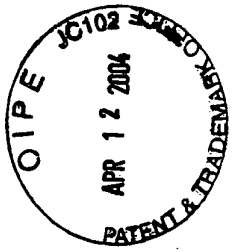
075834.00064 SN09/821,636

MAILING DATE

REFERENCE NUMBER

HOLLAND & KNIGHT LLC

EXPRESS MAIL NO. ET910403511US



PTO/SB/30 (05-03)
Approved for use through 04/30/2003. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Request For Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	09/821,636
Filing Date	March 29, 2001
First Named Inventor	Hiroyuki Ikeda et al.
Art Unit	2811
Examiner Name	Thien F. Tran
Attorney Docket Number	075834.00064

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. ☐ Consider the arguments in the Appeal Brief or Rely Brief previously filed on _____

      ii. ☐ Other _____

   b. ☑ Enclosed

      i. ☑ Amendment/Reply

      ii. ☐ Affidavit(s)/ Declaration(s)

      iii. ☐ Information Disclosure Statement (IDS)

      iv. ☐ Other _____

2. Miscellaneous

   a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

   b. ☐ Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. ☑ The Director is hereby authorized to charge the following fees, or credit any overpayments, to Deposit Account No. 50-1794

      i. ☑ RCE fee required under 37 CFR 1.17(e)

      ii. ☑ Extension of time fee (37 CFR 1.136 and 1.17)

      iii. ☐ Other _____

   b. ☑ Check in the amount of $ 750.00 & $930.00 enclosed

   c. ☐ Payment by credit card (Form PTO-2038 enclosed)

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Robert J. Depke Esq.	*Registration No. (Attorney/Agent)*	37,607
Signature		*Date*	9/19/03

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below. Express Mail No. ET910403511US

Name (Print/Type)	Robert J. Depke Esq.		
Signature		Date	9/19/03

ET 910403511 US

PTO/SB/17 (05-03)
Approved for use through 04/30/2003. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 1,680.00

Complete if Known	
Application Number	09/821,636
Filing Date	March 29, 2001
First Named Inventor	Hiroyuki Ikeda et al.
Examiner Name	Thien F. Tran
Art Unit	2811
Attorney Docket No.	075834.00064

METHOD OF PAYMENT *(check all that apply)*

☑ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 50-1794

Deposit Account Name: HOLLAND & KNIGHT LLP

The Director is authorized to: *(check all that apply)*

☑ Charge fee(s) indicated below ☑ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		X =
Independent Claims		- 3** =		X =
Multiple Dependent				=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	930.00
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	750.00
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 1,680.00

SUBMITTED BY

(Complete *(if applicable)*)

Name *(Print/Type)*	Robert J. Depke	Registration No. *(Attorney/Agent)*	37,607	Telephone	312-263-3600
Signature				Date	9/19/03

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ET 910403511 US

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FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 1,680.00

Complete if Known	
Application Number	09/821,636
Filing Date	March 29, 2001
First Named Inventor	Hiroyuki Ikeda et al.
Examiner Name	Thien F. Tran
Art Unit	2811
Attorney Docket No.	075834.00064

METHOD OF PAYMENT *(check all that apply)*

☑ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 50-1794

Deposit Account Name: HOLLAND & KNIGHT LLP

The Director is authorized to: *(check all that apply)*

☑ Charge fee(s) indicated below ☑ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
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1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	930.00
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	

HOLLAND & KNIGHT LLP 1038785 Commissioner for Patents 09/17/03 CHECK NO. 75008352

VOUCHER NO.	INVOICE NO.	G/L NO.	DESCRIPTION	AMOUNT
1195846	CHI 091703	01104610000000000000000000	75834.64 09/17/03 USPTO Fee for 3 month exte	930.00
			TOTAL	$930.00
			TOTAL	$750.00

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Hiroyuki Ikeda	**Atty. Docket No.**	075834.00064
Serial No.:	09/ 821,636	**Group Art Unit:**	2811
Filed:	March 29, 2001	**Examiner:**	Thien Tran
Invention:	"THIN FILM TRANSISTOR APPARATUS"		

PRELIMINARY AMENDMENT
ACCOMPANYING REQUEST FOR CONTINUED EXAMINATION (RCE)

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

S I R:

In response to the Office Action dated March 19, 2003, please amend the application as follows:

PETITION FOR EXTENSION OF TIME

Applicant hereby petitions for a three month extension of time to respond to the outstanding Office Action under 37 C.F.R. §1.136(a). The time to respond is thus extended to September 19, 2003. Applicant has included a check in the amount of $930.00 as payment of the required fee set forth in 37 C.F.R. §1.17(a).

IN THE CLAIMS:

1. (Currently Amended) A display apparatus comprising:

a plurality of thin film transistors, each of said thin film transistor comprising a semiconductor thin film constituting a channel and having a threshold voltage, and a first gate electrode on one side of said semiconductor thin film and a second gate electrode on an opposite side of said semiconductor thin film,

and further comprising a means for adjusting the threshold voltage by applying a first threshold adjustment voltage to the second gate electrode when the first gate electrode receives a first control voltage and applying a second threshold adjustment voltage to the second gate electrode when the first electrode receives a second control voltage and wherein the voltage applied to the first gate electrode is different from the threshold adjustment voltage applied to the second gate electrode each during voltage application.

2. (Previously Amended) The semiconductor apparatus according to claim 1, wherein said semiconductor thin film constituting said channel is comprised of polycrystalline silicon which does not contain an impurity, and has a thickness of 100 nm or less.

3. (Original) The semiconductor apparatus according to claim 1, wherein said semiconductor thin film constituting said channel is comprised of polycrystalline silicon which contains an impurity effectively affecting the formation of a depletion layer, and has a thickness two times or less the maximum of the thickness of said depletion layer.

4. (Previously Canceled).

5. (Previously Canceled).

Please add the following new claims:

6. (Currently Amended) A liquid crystal display comprising a pair of substrates disposed having a predetermined gap, and a liquid crystal kept in said gap,

one of said substrates containing thereon a display portion in which a pixel electrode and a thin film transistor for driving said pixel electrode are integrated, and a peripheral circuit portion in which thin film transistors are integrated,

the other of said substrates containing thereon an opposite electrode which faces said pixel electrode,

each of said thin film transistors comprising a channel which has a predetermined threshold voltage and on-off operates depending on a gate voltage applied through a wiring, at least a part of said thin film transistors comprising a semiconductor thin film constituting said channel, and a first gate electrode and a second gate electrode, which are disposed on a surface and the other surface of said semiconductor thin film sandwiching an insulating film,

wherein said first gate electrode and said second gate electrode receive a first gate voltage and a second gate voltage, respectively, through wirings which are separately provided,

wherein said first gate electrode. on-off controls said channel depending on said first gate voltage, and wherein said second gate electrode actively controls said threshold voltage depending on said second gate voltage to adjust the on-off operation of said thin film transistors and wherein the voltage applied to the first gate electrode is different from the voltage applied to the second gate electrode during voltage application.

7. (Original) The liquid crystal display according to claim 6, wherein said semiconductor thin film constituting said channel is comprised of polycrystalline silicon which does not contain an impurity effectively affecting the formation of a depletion layer, end has a thickness of 100 nm or less.

8. (Original) The liquid crystal display according to claim 7, wherein, in all of the thin film transistors contained in said display portion and said circuit portion, said semiconductor thin film constituting said channel does not contain an impurity effectively affecting the formation of a depletion layer.

9. (Original) The liquid crystal display according to claim.6, wherein said semiconductor thin film constituting said channel is comprised of polycrystalline silicon which contains an impurity effectively affecting the. formation of a depletion layer, and has a thickness two times or less the maximum of the thickness of said depletion layer.

10. (Original) The liquid crystal display according to claim 9, wherein, in all of. the thin film transistors contained in said display portion and said circuit portion, said semiconductor thin film constituting said channel contains impurity of the same conductive type effectively affecting the formation of a depletion layer.

11. (Original) The liquid crystal display according to claim 6, wherein said second gate electrode actively controls said threshold voltage depending on said second gate voltage applied at least when said thin film transistors off operate, to thereby decrease a current flowing through said, channel when said thin film transistors off-operate, as compared to a current flowing through said channel when said second gate voltage is not applied.

12. (Original) The liquid crystal display according to claim 6, wherein said second gate electrode actively controls said threshold voltage depending on said second gate voltage applied at least when said thin film transistors on operate, to thereby increase a current flowing through said channel when said thin film transistors on-operate, as compared to a current flowing through said channel when said second gate voltage is not applied.

13. (Original) An electroluminescence display comprising a substrate having thereon a display portion in which an electroluminescence device and a thin film transistor for driving said electroluminescence device are integrated, and a peripheral circuit portion in which thin film transistors are integrated,

each of said thin film transistors comprising a channel which has a predetermined threshold voltage and on-off operates depending on a gate voltage applied through a wiring, at least a part of said thin film transistors comprising a semiconductor thin film constituting said channel, and a first gate electrode and a second gate electrode, which are disposed on a surface and a back surface of said semiconductor thin film through an insulating film,

wherein said first gate electrode and said second gate electrode receive a first gate voltage and a second gate voltage, respectively, through wirings which are separately provided,

wherein said first gate electrode on-off controls said channel depending on said first gate voltage, and

wherein said second gate electrode actively controls said threshold voltage depending on said second gate voltage to adjust the on-off operation of said thin film transistors and wherein the voltage applied to the first gate electrode is different from the voltage applied to the second gate electrode during voltage application.

14. (Original) The electroluminescence display according to claim 13, wherein said semiconductor thin film constituting said channel is comprised of polycrystalline silicon which does not contain an impurity effectively affecting the formation of a depletion layer, and has a thickness of 100 nm or less.

15. (Original) The electroluminescence display according to claim 14, wherein, in all of the thin film transistors contained in said display portion and said circuit portion, said semiconductor thin film constituting said channel does not contain an impurity effectively affecting the formation of a depletion layer.

16. (Original) The electroluminescence display. according to claim 13, wherein said semiconductor thin film constituting said channel is comprised of polycrystalline silicon which contains an impurity effectively affecting the formation of a depletion layer, and has a thickness two times or less the maximum of the thickness of said depletion layer.

17. (Original) The electroluminescence display according to claim 16, wherein, in all of the thin film transistors contained in said display portion and said circuit portion, said semiconductor thin film constituting said channel contains impurity of the same conductive type effectively affecting the formation of a depletion. layer.

18. (Original) The electroluminescence display according to claim 13, wherein said second gate electrode actively controls said threshold voltage depending on said second gate voltage applied at least when said thin film transistors off-operate, to thereby decrease a current flowing through said channel when said thin film transistors off operate, as compared to a current flowing through said channel when said second gate voltage is not applied.

19. (Original) The electroluminescence display according to claim 13, wherein said second gate electrode actively controls said threshold voltage depending on said second gate voltage applied at least when said thin film transistors on-operate, to thereby increase a current flowing through said channel when said thin film transistors on-operate, as compared to a current flowing through said channel when said second gate voltage is not applied.

Please add the following new claim:

20. (Newly Added) A display apparatus comprising:

a plurality of thin film transistors, each of said thin film transistor comprising a semiconductor thin film constituting a channel and having a threshold voltage, and a first gate electrode above said semiconductor thin film and a second gate electrode below said semiconductor thin film,

and further comprising a means for adjusting the threshold voltage by applying a first threshold adjustment voltage to the second gate electrode when the first gate electrode receives a first control voltage and applying a second threshold adjustment voltage to the second gate electrode when the first electrode receives a second control voltage and wherein the voltage applied to the first gate electrode is different from the threshold adjustment voltage applied to the second gate electrode during voltage application.

REMARKS

Applicant has herein modified the claims to more specifically define the invention. Applicant submits that the prior art provides no teaching or suggestion whatsoever regarding the claimed distinct voltages applied to the first and second gate electrodes.

Respectfully submitted,

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(Reg. #37,607)

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Inventor(s):	Hiroyuki Ikeda
Our Case No.	075834.00064
	Express Mail Certificate, Request for Continued Examination Transmittal, Fee Transmittal, Preliminary Amendment With Three Month Time Extension Request Accompanying Request for Continued Examination
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